REMARKS

This Amendment is filed in response to the first Office Action dated January 15, 2004, which has a shortened statutory period set to expire April 15, 2004.

Claims 37-53 and 55-58 Are Directed To Statutory Subject Matter

Applicants respectfully traverse the rejection of Claims 37-53 and 55-58 under 35 U.S.C. 101. Claim 37 now recites a "memory model usable for simulation and automatic test pattern generation". Claim 51 now recites a "content addressable memory model usable for simulation and automatic test pattern generation". Claim 53 now recites a "combined content addressable memory (CAM) and random access memory (RAM) model usable for simulation and automatic test pattern generation". Claim 55 recites a "memory model compatible with a simulation tool and an automatic test pattern generation (ATPG) tool".

These recitations clearly indicate a "useful, concrete, and tangible" purpose that satisfies the statutory subject matter requirement of 35 U.S.C. 101. As taught by Applicants, these recited memory models have significant advantages. For example, Applicants' recited memory models are constructed directly from behavioral descriptions. Thus, the tedious, time-consuming, error-prone, and difficult tasks of manually re-coding ATPG models for memories and verifying functional equivalence between simulation models and ATPG models can be eliminated. Specification, page 5, lines 6-11. Moreover, such memory models can be easily debugged using a schematic viewer. Specification, page 6, lines 15-20.

Applicants also direct the Examiner's attention to the article cited in the Office Action and written by the inventors of the present application, "Using Verilog Simulation Libraries For ATPG". In this article, the Abstract explicitly states,

> Significant engineering effort is invested in coding libraries for automatic test pattern generation (ATPG) and verifying their equivalence with corresponding "golden" simulation libraries.

In this article, the Introduction further states,

> After significant effort is expended into creating this "golden" simulation library, a secondary "ATPG library" is created to support rules checking and automatic test generation. This only-for-test library must then be verified against the golden simulation library, which is an engineering time-consuming process. The difficulty stems from the fact that the two libraries are written in two very different languages and styles: the simulation library may contain structural, register-transfer and behavioral constructs, as well as timing and other information. The test library, by contrast, is purely structure, optimized for ATPG and has no timing. The test library and netlists read are combined to build an internal APTG model that all ATPG rules refer to. This model may differ significantly from the simulation library that the designers are accustomed to, making debug of test problems difficult.

Thus, this article confirms that Applicants' recited models eliminate the coding and verifying of the separate ATPG library and simplify debugging (compare Figures 1 and 2 of this article). Based on the above reasons, Applicants request reconsideration and withdrawal of the rejection of Claims 37, 51, 53, and 55.

Claims 38-50 depend from Claim 37 and therefore are patentable for at least the reasons presented for Claim 37. Claim 52 depends from Claim 51 and therefore is patentable for at least the reasons presented for Claim 51. Claims 56-58 depend from Claim 55 and therefore are patentable for at least the reasons presented for Claim 55. Based on the above reasons, Applicants request reconsideration and withdrawal of the rejection of Claims 38-50, 52, 56-58.

Applicants Have Overcome The Rejections Under 35 U.S.C. 102

Applicants submit herewith a Call For Papers for the International Test Conference in 1999. As noted in this document, the International Test Conference started on September 28, 1999. This application was filed on July 23, 1999. Therefore, the article "Using Verilog Simulation Libraries For ATPG", which was presented at the 1999 International Test Conference, is not prior art and cannot be used to reject Applicants' claims.

Applicants note for the record that Claims 51-53 and 55-58 recite limitations regarding a CAM model and a combined CAM-RAM model. These models are neither disclosed nor suggested by the article "Using Verilog Simulation Libraries For ATPG".

Based on the above reasons, Applicants request reconsideration and withdrawal of the rejection of Claims 37-53 and 55-58 under 35 U.S.C. 102(a).

Applicants Have Overcome The Rejection Under 35 U.S.C. 112

The term "for coupling to" refers to the relationship between primitives. Specifically, primitives are not actual components that are connected or coupled. Instead, primitives have coupling relationships that form the model. During the EDA process, the user can quantize these coupling relationships, thereby transforming the model into an actual memory for a circuit.

Applicants are unaware as to why "A coupled to B" should mean that the signal(s) flow from A to B. Applicants would appreciate if the Examiner could cite the MPEP section or other guide that provides this interpretation.

Applicants have amended the claims to clarify the coupling relationship between the primitives. Specifically, the independent claims now recite specific ports for the recited

primitives, e.g. input, output, write_address, and read_data ports.

Applicants direct the Examiner's attention to Figures 6A and 10 for exemplary memory models that correspond to the claims. Applicants submit that no further figures are needed.

In light of the explanation of terminology and the clarifications to the claims, Applicants submit that Claims 37-53 and 55-58 point out and distinctly claim the subject matter that Applicants regard as the invention. Moreover, Applicants submit that Claims 37-53 and 55-58 contain subject matter that was described in the specification in such a way as to enable one skilled in the art to make and/or use the invention.

Based on the above reasons, Applicants request reconsideration and withdrawal of the rejection of Claims 37-53 and 55-58 under 35 U.S.C. 112 (first and second paragraphs).

CONCLUSION

Claims 37-53 and 55-58 are pending in the present application. Applicants request allowance of these claims.

If the next action is other than allowance, please telephone the undersigned at 408-451-5907 to schedule a telephone interview.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as FIRST CLASS MAIL in an envelope addressed to: Mail Stop Non-Fee Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on April 1, 2004.

4/1/2004 Rebecca A. Baumann
Date Signature: Rebecca A. Baumann